DS1747/DS1747P
Y2K-Compliant, Nonvolatile Timekeeping RAMs

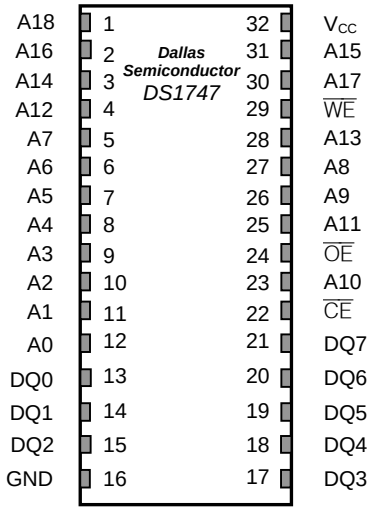
FEATURES

- **Integrated NV SRAM, Real-Time Clock (RTC), Crystal, Power-Fail Control Circuit, and Lithium Energy Source**
- **Clock Registers are Accessed Identically to the Static RAM. These Registers are Resident in the Eight Top RAM Locations**
- **Century Byte Register (Y2K Compliant)**
- **Totally Nonvolatile with Over 10 Years of Operation in the Absence of Power**
- **BCD-Coded Century, Year, Month, Date, Day, Hours, Minutes, and Seconds with Automatic Leap Year Compensation Valid Up to the Year 2100**
- **Battery Voltage-Level Indicator Flag**
- **Power-Fail Write Protection Allows for ±10% V_{CC} Power-Supply Tolerance**
- **Lithium Energy Source is Electrically Disconnected to Retain Freshness Until Power is Applied for the First Time**
- **DIP Module Only:**
  Standard JEDEC Byte-Wide 512k x 8 Static RAM Pinout
- **PowerCap® Module Board Only:**
  Surface-Mountable Package for Direct Connection to PowerCap Containing Battery and Crystal
  Replaceable Battery (PowerCap)
  Power-On Reset Output
  Pin-for-Pin Compatible with Other Densities of DS174xP Timekeeping RAM
- **Also Available in Industrial Temperature Range: -40°C to +85°C**

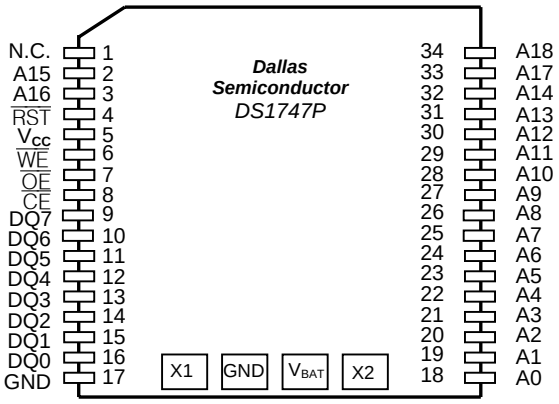
PowerCap is a registered trademark of Dallas Semiconductor Corp.

PIN CONFIGURATIONS

TOP VIEW



Encapsulated DIP
(512k x 8)



PowerCap Module Board
(Uses DS9034PCX PowerCap)

ORDERING INFORMATION

PART	SUPPLY VOLTAGE (V)	TEMP RANGE	PIN-PACKAGE	TOP MARK†
DS1747-70	5.0	0°C to +70°C	32 EDIP (0.740a)	DS1747-70
DS1747-70IND	5.0	-40°C to +85°C	32 EDIP (0.740a)	DS1747-70 IND
DS1747P-70	5.0	0°C to +70°C	34 PowerCap*	DS1747P-70
DS1747P-70IND	5.0	-40°C to +85°C	34 PowerCap	DS1747P-70 IND
DS1747W-120	3.3	0°C to +70°C	32 EDIP (0.740a)	DS1747W-120
DS1747W-120IND	3.3	-40°C to +85°C	32 EDIP (0.740a)	DS1747W-120 IND
DS1747WP-120	3.3	0°C to +70°C	34 PowerCap*	DS1747WP-120
DS1747WP-120IND	3.3	-40°C to +85°C	34 PowerCap*	DS1747WP-120 IND
DS1747-70+	5.0	0°C to +70°C	32 EDIP (0.740a)	DS1747-70
DS1747-70IND+	5.0	-40°C to +85°C	32 EDIP (0.740a)	DS1747-70 IND
DS1747P-70+	5.0	0°C to +70°C	34 PowerCap*	DS1747P-70
DS1747P-70IND+	5.0	-40°C to +85°C	34 PowerCap*	DS1747P-70 IND
DS1747W-120+	3.3	0°C to +70°C	32 EDIP (0.740a)	DS1747W-120
DS1747W-120IND+	3.3	-40°C to +85°C	32 EDIP (0.740a)	DS1747W-120 IND
DS1747WP-120+	3.3	0°C to +70°C	34 PowerCap*	DS1747WP-120
DS1747WP-120IND+	3.3	-40°C to +85°C	34 PowerCap*	DS1747WP-120 IND

**DS9034PCX, DS9034I-PCX, DS9034PCX+, DS9034I-PCX required (must be ordered separately).*
†A "+" indicates a lead free. The top mark will include a "+" symbol on lead-free devices.

DESCRIPTION

The DS1747 is a full-function, year-2000-compliant (Y2KC), real-time clock/calendar (RTC) and 512k x 8 nonvolatile static RAM. User access to all registers within the DS1747 is accomplished with a byte-wide interface as shown in Figure 1. The RTC information and control bits reside in the eight uppermost RAM locations. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour binary-coded decimal (BCD) format. Corrections for the date of each month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1747 also contains its own power-fail circuitry that deselects the device when the V_{CC} supply is in an out-of-tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.3V to +6.0V
Operating Temperature Range (Noncondensing)..……...0°C to +70°C (Commercial)
……..……-40°C to +85°C (Industrial)
Storage Temperature Range……...-40°C to +85°C
Soldering Temperature (EDIP) (Leads, 10 seconds) (Note 7)……..+260°C
Soldering Temperature (Note 7)…….See IPC/JEDEC Standard J-STD-020 for Surface-Mount Devices

This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = Over the Operating Range)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1 Voltage All Inputs	V_{CC} = 5V±10%	V_{IH}	2.2		V_{CC} + 0.3V	V	1
	V_{CC} = 3.3V±10%	V_{IH}	2.0		V_{CC} + 0.3V	V	1
Logic 0 Voltage All Inputs	V_{CC} = 5V±10%	V_{IL}	-0.3		+0.8	V	1
	V_{CC} = 3.3V±10%	V_{IL}	-0.3		+0.6	V	1

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	Icc			85	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH})	Icc_1			6	mA	2, 3
CMOS Standby Current ($\overline{CE}$ ≥ V_{CC} - 0.2V)	Icc_2			4	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} = +2.1mA)	V_{OL}			0.4		1
Write Protection Voltage	V_{PF}	4.25		4.50	V	1
Battery Switchover Voltage	V_{SO}		V_{BAT}			1, 4

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	Icc			30	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH})	Icc_1			2	mA	2, 3
CMOS Standby Current ($\overline{CE}$ ≥ V_{CC} - 0.2V)	Icc_2			2	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} = +2.1mA)	V_{OL}			0.4		1
Write Protection Voltage	V_{PF}	2.80		2.97	V	1
Battery Switchover Voltage	V_{SO}		V_{BAT} or V_{PF}		V	1, 4

AC CHARACTERISTICS—READ CYCLE (5V)

(V_{CC} = 5.0V ±10%, T_A = Over the Operating Range.)

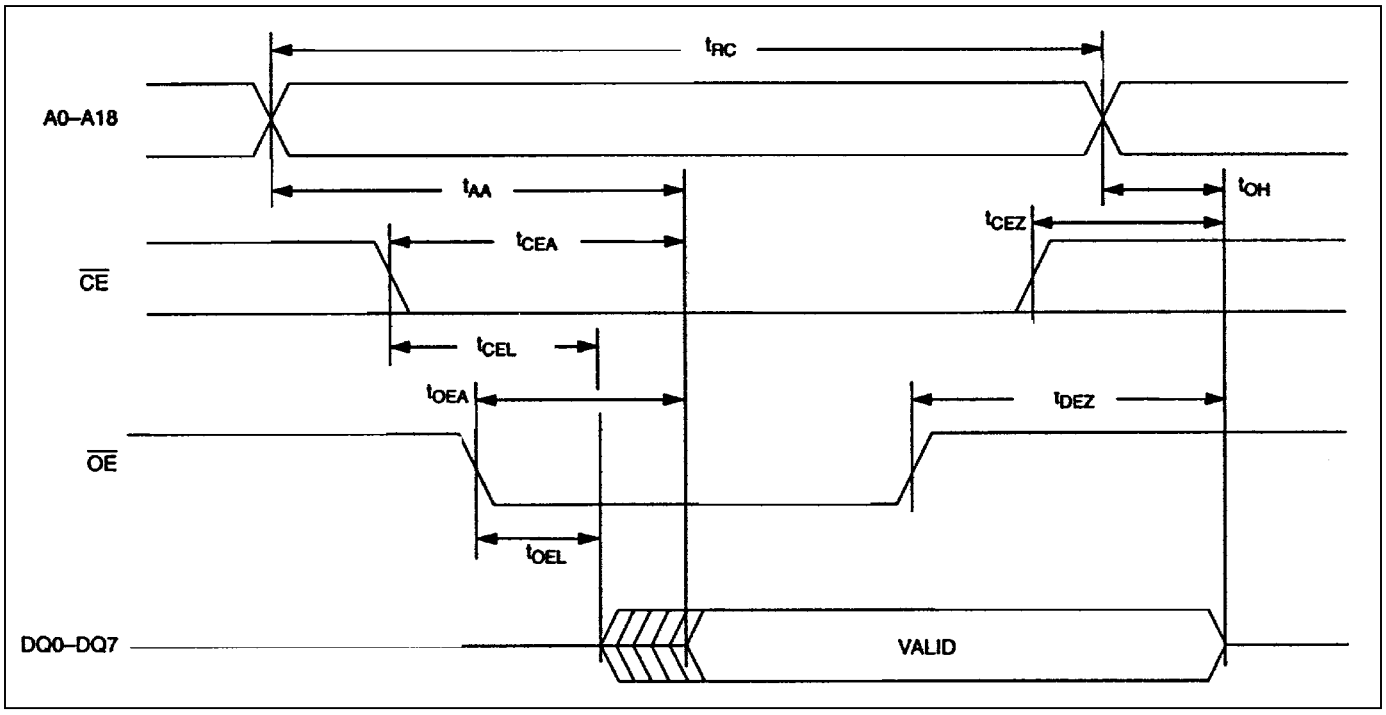
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	70			ns	
Address Access Time	t_{AA}			70	ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5			ns	
$\overline{CE}$ E Access Time	t_{CEA}			70	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}			25	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5			ns	
$\overline{OE}$ Access Time	t_{OEA}			35	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}			25	ns	
Output Hold from Address	t_{OH}	5			ns	

AC CHARACTERISTICS—READ CYCLE (3.3V)

(V_{CC} = 3.3V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
Address Access Time	t_{AA}			120	ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5			ns	
$\overline{CE}$ E Access Time	t_{CEA}			120	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}			40	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5			ns	
$\overline{OE}$ Access Time	t_{OEA}			100	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}			35	ns	
Output Hold from Address	t_{OH}	5			ns	

READ CYCLE TIMING DIAGRAM



AC CHARACTERISTICS—WRITE CYCLE (5V)

(V_{CC} = 5.0V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	70			ns	
Address Setup Time	t_{AS}	0			ns	
$\overline{WE}$ Pulse Width	t_{WEW}	50			ns	
$\overline{CE}$ Pulse Width	t_{CEW}	60			ns	
Data Setup Time	t_{DS}	30			ns	
Data Hold Time	t_{DH1}	0			ns	8
Data Hold Time	t_{DH2}	0			ns	9
Address Hold Time	t_{AH1}	5			ns	8
Address Hold Time	t_{AH2}	5			ns	9
$\overline{WE}$ Data Off Time	t_{WEZ}			25	ns	
Write Recovery Time	t_{WR}	5			ns	

AC CHARACTERISTICS—WRITE CYCLE (3.3V)

(V_{CC} = 3.3V ±10%, T_A = Over the Operating Range.)

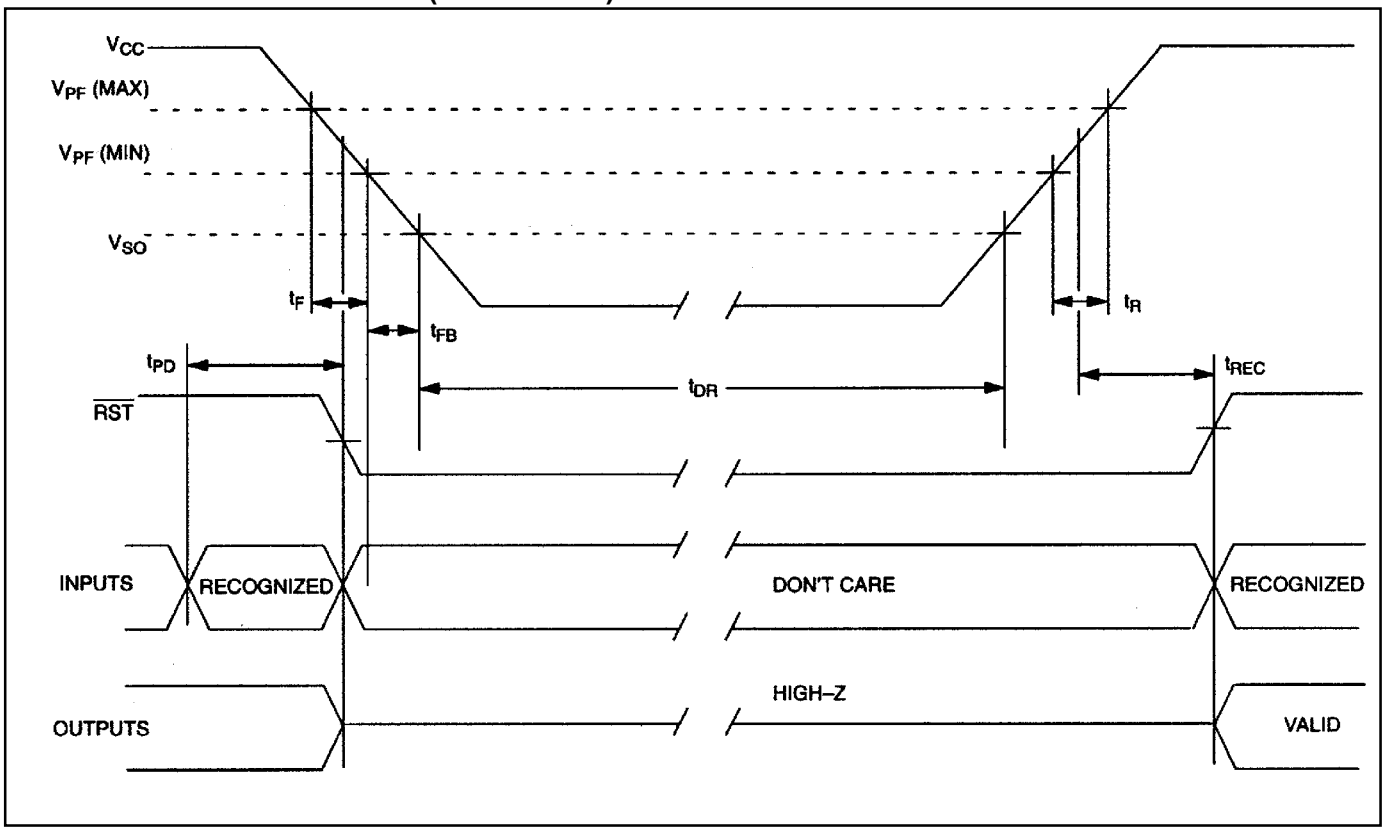
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	120			ns	
Address Setup Time	t_{AS}	0		120	ns	
$\overline{WE}$ Pulse Width	t_{WEW}	100			ns	
$\overline{CE}$ Pulse Width	t_{CEW}	110			ns	
$\overline{CE}$ and CE2 Pulse Width	t_{CEW}	110			ns	
Data Setup Time	t_{DS}	80			ns	
Data Hold Time	t_{DH1}	0			ns	8
Data Hold Time	t_{DH2}	0			ns	9
Address Hold Time	t_{AH1}	0			ns	8
Address Hold Time	t_{AH2}	10			ns	9
$\overline{WE}$ Data Off Time	t_{WEZ}			40	ns	
Write Recovery Time	t_{WR}	10			ns	

POWER-UP/DOWN AC CHARACTERISTICS (5V)

(V_{CC} = 5.0V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_H Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Fall Time: $V_{PF(MIN)}$ to V_{SO}	t_{FB}	10			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$) to $V_{PF(MAX)}$	t_R	0			µs	
Power-Up Recover Time VPF to $\overline{RST}$ High (PowerCap Only)	t_{REC}			35	ms	
Expected Data-Retention Time (Oscillator ON)	t_{DR}	10			years	5, 6

POWER-UP/DOWN TIMING (5V DEVICE)

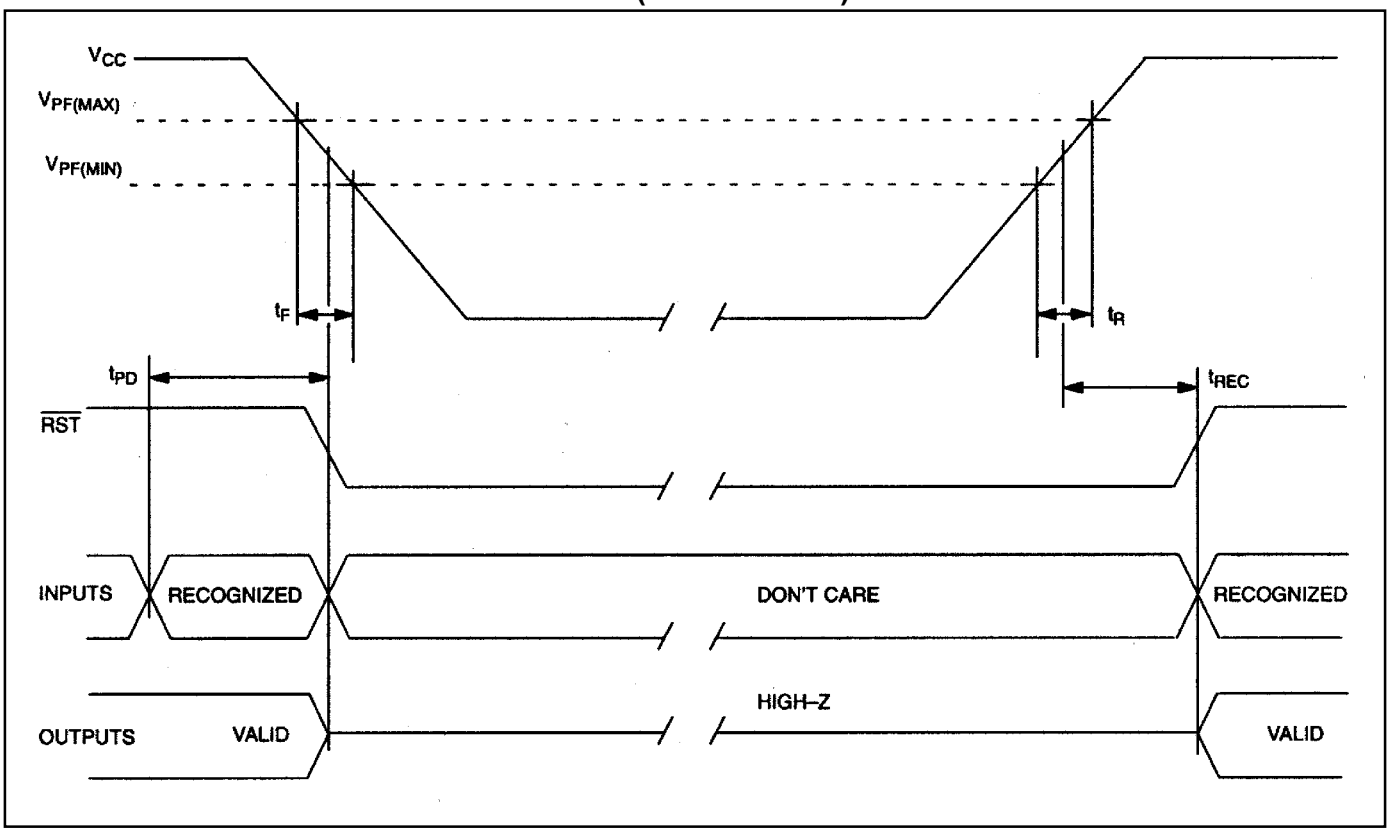


POWER-UP/DOWN CHARACTERISTICS (3.3V)

(V_{CC} = 3.3V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_H, Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
Power-Up Recover Time V_{PF} to $\overline{RST}$ High (PowerCap Only)	t_{REC}			35	ms	
Expected Data-Retention Time (Oscillator ON)	t_{DR}	10			years	5, 6

POWER-UP/DOWN WAVEFORM TIMING (3.3V DEVICE)



CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on All Input Pins	C_{IN}			14	pF	
Capacitance on All Output Pins	C_O			10	pF	

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0 to 3.0V
Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

NOTES:

1) Voltages are referenced to ground.
2) Typical values are at +25°C and nominal supplies.
3) Outputs are open.
4) Battery switchover occurs at the lower of either the battery terminal voltage or V_{PF}.
5) Data-retention time is at +25°C.
6) Each DS1747 has a built-in switch that disconnects the lithium source until the user first applies V_{CC}. The expected t_{DR} is defined for DIP modules and assembled PowerCap modules as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
7) RTC encapsulated DIP (EDIP) modules can be successfully processed through conventional wave-soldering techniques as long as temperatures as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water-washing techniques is acceptable, provided that ultra-sonic vibration is not used.
8) t_{AH1}, t_{DH1} are measured from $\overline{WE}$ going high.
9) t_{AH2}, t_{DH2} are measured from $\overline{CE}$ going high.